

## VOLTAGE BALANCE CONTROL OF TWO-LEVEL DC-DC CONVERTER

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**Abstract.** The multilevel DC-DC converters have advantages of low voltage stress of the switches and diodes and reduction of the filter size. Therefore, such converters are becoming more popular in wide range of application. While multilevel topology offers many new features, it also necessitates a balance control of the capacitors. In the paper a method of capacitor voltage balancing for multilevel isolated DC-DC converters is proposed. The voltage balancing analysis is carried out for a two level converter with input series output parallel structure. The paper describes the operating principles of the balancing circuit, analyzes the fundamental relationships and compares this method with the traditional ones.

**Keywords:** DC-DC converter, multilevel converter, voltage balancing

### Introduction

In high and medium voltage application, the multilevel converters are a good choice for AC-DC, DC-AC or DC-DC conversion as in such converters the voltage across the semiconductors is reduced and therefore MOSFET transistors instead of IGBT can be used having better switching and conduction performance compared to the switches rated on the full blocking voltage. Therefore, the overall performance of the converter, including the cost and efficiency, can be better compared to conventional topology of converters. Often the voltage of the DC bus is divided by using a capacitive voltage divider. For some reasons voltage of the capacitors can change, for example, during the start of the converter, variations of input voltage, light difference between the drive signals of the switches or due to the difference of the characteristics for each individual component. As a result, the voltage on transistor switches can increase to an unsafe value. Therefore, balance control is necessary to connect individual loads at each capacitor, in order to discharge them and to balance the capacitor voltages. The capacitors must have their voltages balanced at nominal value for proper operation of the converter.

Most multilevel topologies are balanced by using the active voltage balancing strategy [1-5] that consists of a voltage balancing control loop incorporated in the main control system. Such a voltage balance control system can be implemented in the multilevel converters only if digital control of the converter is used. Furthermore, this control loop additionally requires calculation capacity of the microcontroller or FPGA. The control system becomes complicated and more expensive. An analogue control method has fast response, precision, better resolution, so it remains still attractive in many applications. In this paper a scheme that allows balancing voltage without digital appliances is proposed.

### Theoretical analysis

Figure 1 shows a simple capacitive voltage divider that is used to obtain two voltage levels. If the system is balanced, the voltage of the capacitor is equal to  $V_{IN}/2$  and the current  $i_N$  is zero.

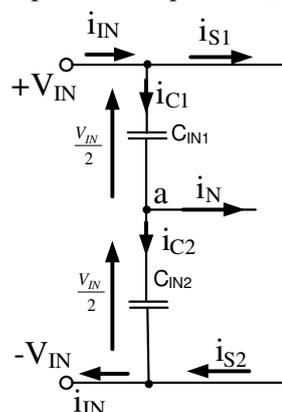


Fig. 1. Simplified circuit of the voltage divider used in theoretical analysis

To understand the capacitor voltage behavior it is necessary to study the capacitor current while the capacitor voltage and current are directly related. Analyzing the current through the capacitors of the circuit shown in Fig. 1, the following equations can be obtained:

$$i_{C1} = i_{IN} - i_{S1}, \quad (1)$$

$$i_{C2} = i_{IN} - i_{S2}, \quad (2)$$

$$i_N = i_{C1} - i_{C2}, \quad (3)$$

$$i_{C1} = C_{IN1} \frac{dv_{C1}}{dt}. \quad (4)$$

By substitution (4) into (3), it is obtained:

$$i_N = C_1 \cdot \frac{dv_{C1}}{dt} - C_2 \frac{dv_{C2}}{dt}. \quad (5)$$

As the input voltage is the sum of the capacitor voltages, it follows:

$$\frac{dV_{IN}}{dt} = \frac{dv_{C1}}{dt} + \frac{dv_{C2}}{dt}. \quad (6)$$

The input voltage is considered constant, free of oscillations, so its derivative is equal to zero, then the equation (6) can be simplified:

$$\frac{dv_{C1}}{dt} = - \frac{dv_{C2}}{dt}. \quad (7)$$

Considering  $C_1 = C_2$  and replacing (7) in (6), the relationship is obtained between  $i_N$  and  $v_{C1}$ , as follows:

$$i_N = 2C_1 \frac{dv_{C1}}{dt}. \quad (8)$$

By rearranging of (8), we obtain:

$$\frac{dv_{C1}}{dt} = \frac{i_N}{2C_1}. \quad (9)$$

On the other hand, current  $i_N$  can be expressed through the load current as follows:

$$i_N = i_{S2} - i_{S1}. \quad (10)$$

From these equations it can be concluded that the difference in currents through transistors ( $i_{S1}, i_{S2}$ ) causes misbalance of the capacitors voltage. As the feedback system regulates the load current, this current can be considered as unchanged through the switching period. The difference of currents of both legs  $i_{S1}, i_{S2}$  can be called unequal inductance of the inductors, transformers, unlike parameters of semiconductors or different duty cycle, especially in the transient process.

Misbalance in the voltage causes larger current in the leg with higher voltage, so a slow process of stabilization will take place but mostly it is not enough to hold the voltage of the capacitor in the desired level. Therefore, some solution is necessary to prevent the situation when the voltage of the capacitor reaches a dangerous value and damages semiconductors or passive elements. The solution must compensate current  $i_N$  thus preventing misbalance of the capacitor voltages. The scheme must be sufficiently simple with as small as possible power losses.

### The passive voltage balancing

The simplest method to balance voltages of the capacitors is using a voltage divider, which consists of two resistors  $R_B$ , such circuit is shown in Figure 2. For practical application the value of these resistors must be selected such that the expected misbalance current  $i_N$  is small in comparison to the current through the resistors by equal voltages on the capacitors  $i_{divider}$  to achieve voltage deviation  $\Delta U$  as close as possible to zero. Even more, the resistors  $R_B$  must be selected taking into account the worst-case misbalance current  $i_N$ . If the actual value of  $i_N$  is smaller, losses in the balancing resistors

still remain permanently high. As differences of the leakage currents of the both capacitances are small ( $i_{C1} \approx i_{C2}$ ) in comparison to the misbalance current  $i_N$ , it follows:

$$i_N = i_{compensation} \cdot \tag{11}$$

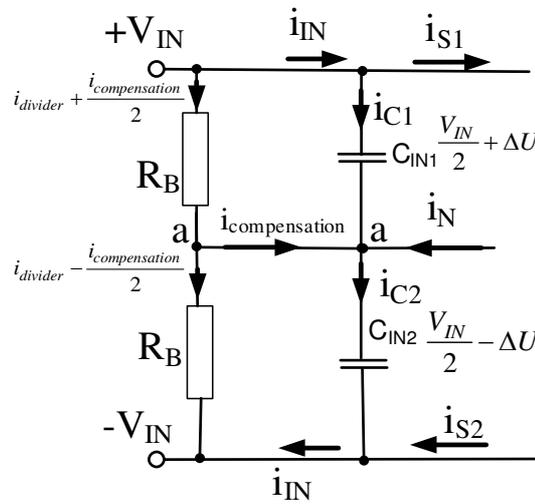


Fig. 2. Passive voltage balancing circuit

The voltage deviation of the capacitor can be expressed as follows:

$$\Delta V = \frac{1}{2} \cdot i_{compensation} \cdot R_B = \frac{1}{2} \cdot i_N \cdot R_B \tag{12}$$

The normalized deviation by the nominal voltage  $V_{IN}/2$  of the capacitors is equal to:

$$\Delta v = \frac{\Delta V}{\frac{1}{2} V_{IN}} = \frac{\frac{1}{2} i_N R_B}{i_{divider} \cdot R_B} = \frac{1}{2} \frac{i_N}{i_{divider}} \tag{13}$$

If the deviation of the voltage of the capacitor  $\Delta v$  shall be less than 20 percent not to breakdown transistors and capacitors, a value of the  $R_B$  has to be selected to ensure  $i_{divider} > 2.5 i_N$ . Then the losses of the balancing resistors can be calculated as:

$$P_B = 2 \cdot i_{divider}^2 \cdot R_B + \frac{R_B}{2} \cdot i_N^2 = 2 \cdot R_B \cdot i_{divider}^2 (1 + \Delta v^2) \tag{14}$$

The misbalance current  $i_N = 100$  mA at  $V_{IN} = 600$  V DC results in balancing losses of  $P_B = 156$  W. If the converter is used, often it leads to very large losses of the electrical energy. This suggests the development of an advanced balancing method.

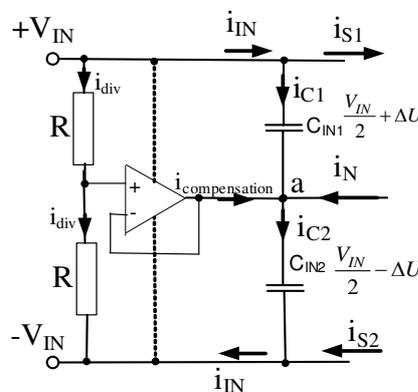


Fig. 3. Active voltage balancing

The active balancing method shown in Figure 3 and proposed in [6] allows to avoid permanent losses in the resistors, the losses of the active balancing can be calculated:

$$P_{balancing} = \frac{1}{2} \cdot V_{IN} \cdot i_N \quad (15)$$

But still losses remain high as the input voltage is high, additionally, this balancing circuit requires a high-voltage operational amplifier which is expensive.

### The proposed balancing method

In this paper, the voltage balancing circuit for the input series-output parallel connected converter configuration is shown in Figure 5 for medium-voltage power conversion applications but such circuit can be used in other isolated configurations, too. The input-series output-parallel (ISOP) configuration consists of two modular DC-DC converters connected in series at the input and in parallel at the output, enabling the use of high switching frequency metal oxide semiconductor field effect transistors (MOSFETs) with low voltage ratings, which leads to a high power density and a high conversion efficiency. As the output current ripple frequency is twice of the switching frequency, which is shown in Figure 5, the size and costs of the output filter can be reduced. The control of the converter is realized by using the analogue circuit realized in an analogue chip.

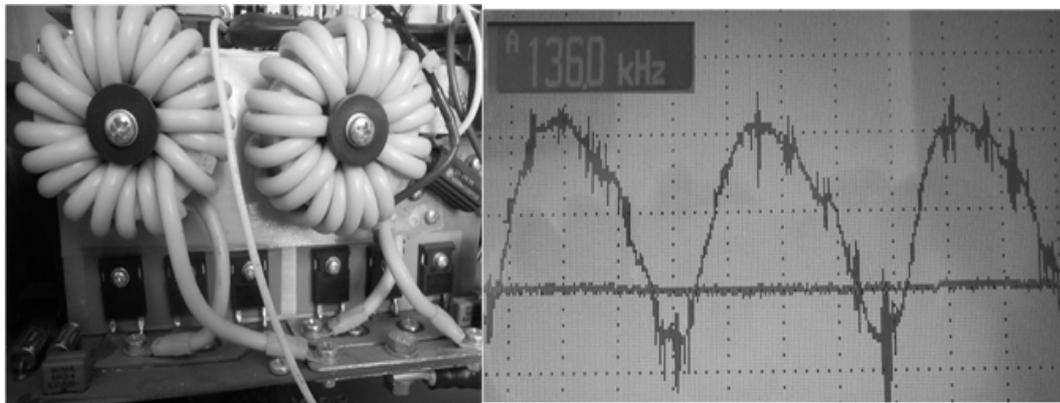


Fig. 5. DC-DC converter and current in the inductor

Figure 6 shows basic schematic of the converter and balancing circuit. The balancing circuit consists of an additional winding of the transformer with number of windings equal to the number of the windings of the primary side of the pulse transformer. In the series with this winding the resistor  $R_1$  is connected, which limits the balancing current and diode  $VD_3$  to prevent power losses in the resistor if the voltage of the capacitor is higher than of the balancing winding.

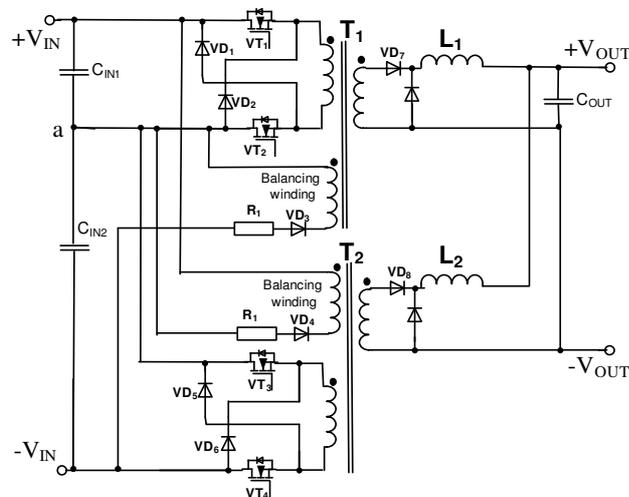


Fig. 6. Input series output parallel dc-dc converter with balancing circuit

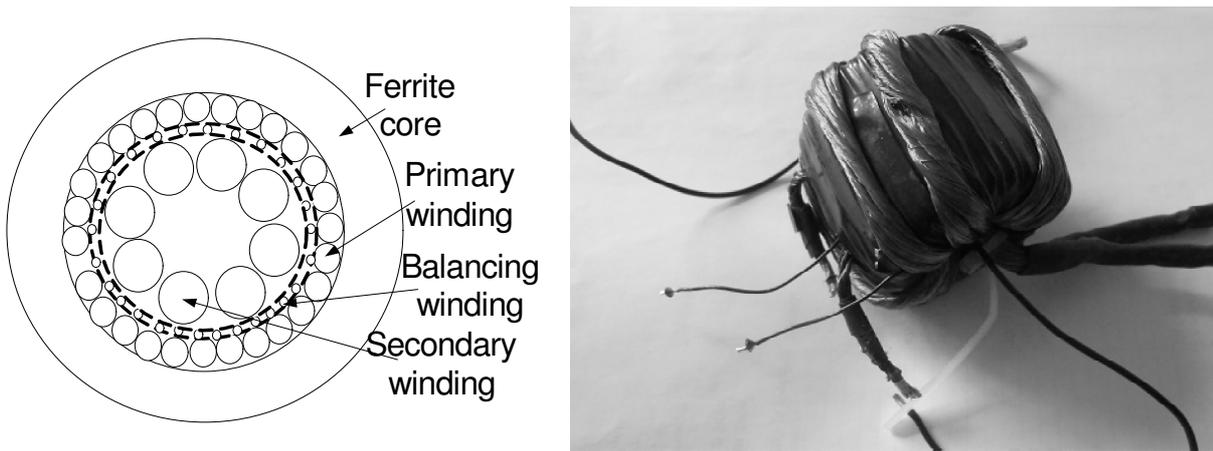


Fig. 7. Transformer with integrated balancing winding

Figure 7 shows the structure of the proposed transformer, which consists of a round ferrite core and three windings. The number of turns of the secondary winding and balancing winding are equal to 27. For the balancing winding a wire with the cross sectional area equal to 0,2 mm<sup>2</sup> is used. For the secondary winding litz wire with cross sectional area equal to 7 mm<sup>2</sup> is used.

Figure 8 explains the operational principle of the proposed circuit. If the voltage of the capacitor is higher than that of the balancing winding, the current of the corresponding transistor flows from the balancing winding to the capacitor and partly compensates the current  $i_N$  thus gradually equalizing the voltage levels of the both capacitors. The voltage levels can not be equalized to equal values but it is not necessary in this case as the main task of the balancing is to prevent dangerous values of the voltage, additionally, there is realized a circuit that switches off the converter if the voltage of one of the capacitors becomes critically high.

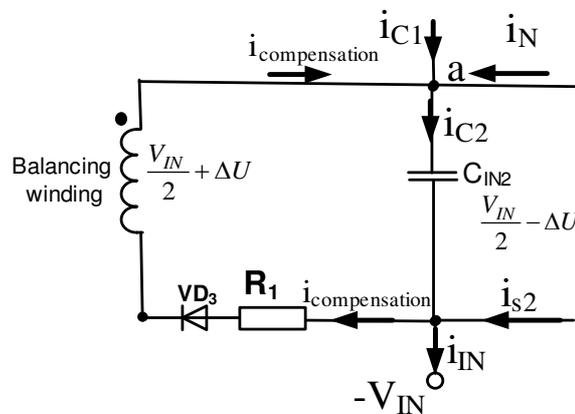


Fig. 8. Operational principle of the balancing circuit

The power losses in the resistor can be expressed as follows:

$$P_{balancing} < 2 \cdot \Delta U \cdot i_N . \tag{16}$$

The power losses in this circuit in comparison to the previous ones are significantly lower, therefore, the compact balancing resistor can be used with power of several watts, additional balancing windings can be created by using a wire with a small cross-sectional area.

The experimental results demonstrate that the voltage of both capacitors in all operating modes stays ideally equal; therefore these oscillograms are not presented in the paper. The measured temperature of the balancing resistors is less than 45 degrees Celsius. This means that balancing losses are small and the proposed method is suitable for practical applications. Of course, it would be necessary to test the balancing circuit in a longer time period; therefore, in practical applications it is advisable to use an additional protective circuit against overvoltage of the capacitors.

## Conclusions

The voltage balancing of the capacitors of the multilevel converter can be big challenge. In the paper a method to solve this problem without implementation of the digital control is proposed. The circuit is simple and cheap, it allows prevent rising of the capacitor voltage to the dangerous voltage with negligible power losses. The proposed circuit is useful for the isolated multilevel converter.

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