PULSE DENSITY MODULATION CIRCUIT

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Abstract. The research paper discusses the principles of the pulse density modulation control circuit design. The article provides a separate mathematical analysis of circuit components such as non-inverting amplifier operation, its circuits, capacitor charging/discharging and integrator reset circuits and operation. Also simulation results are given and the circuit test bench has being built.

Keywords: Pulse density modulation circuit, power converter control circuit, integrator reset circuit, non-inverting amplifier.

Introduction

The pulse density modulation (PDM) circuit is related to power converters and can be used in power electronics. The aim of the pulse density modulation circuit design and application in power electronics is to improve AC formation precision and quality parameters. The pulse density modulation control circuit design is based on operational amplifiers (OP). Mainly the circuit consists of the signal generator SG, integrating operational amplifier, RC contour with the charge capacitor C1, charge/discharge control unit with the capacitor discharge switch, integrator blocking unit and differentiator of output pulses. The circuit is designed to modulate sine curve form. The voltage level of the signal generator SG on input of the circuit determines the capacitor C1 charge speed, and this capacitor voltage is compared with voltage Uref that is less than the integrator feed voltage and is related to it. The point when the capacitor voltage reaches Uref determines the beginning of pulse on the circuit output and the capacitor discharge switch is activated, the point when the capacitor voltage reaches 0V determines the end of the pulse on circuit output. After the capacitor discharge switch is deactivated the discharge circuit is interrupt. Now the new cycle is beginning and the capacitor C1 is being charged again. This way the pulse density modulation circuit is achieved, which generates fewer constant length pulses at lower input voltage. Increasing the input voltage, the output pulse count per time unit on circuit output increases, in addition the pulse length remains fixed. Every output pulse blocks the input signal at its corresponding moment to escape capacitor charging and discharging simultaneously. Output pulses are differenced to the desired amplitude so PDM circuit is suitable for use as a power electronics control circuit.

Materials and methods

The block diagram of the designed circuit is shown in Fig. 1. The aim is to create a pulse density modulation circuit, that does conversion of the input signal into constant length pulse packet and the pulse density depends on the input signal voltage level.

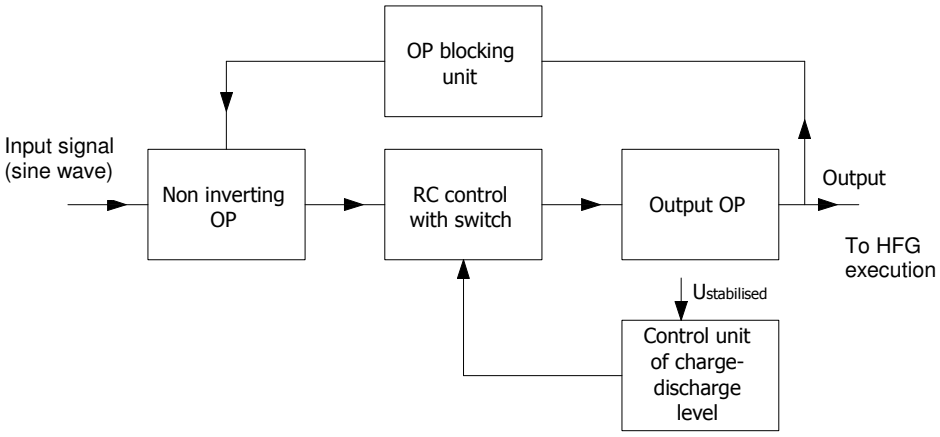

Fig. 1. **Pulse density modulation circuit block diagram**

The purpose of the designed circuit is to use it to control power inverters. Therefore, mathematic analysis is performed for components that are used in this circuit (Fig. 1), such as non inverting integrator, exponential signal generator and integrator reset unit. The pulse density circuit operating principle is that the input signal is integrated into the integration of capacity, up to a certain voltage level. In the moment when the integrating capacitor voltage reaches this voltage level, the discharge switch is opened, while the capacitor is being discharged the circuit outlet forms a pulse. After the capacitor is discharged it is being charged again.

Non-inverting amplifier. [2] The basic circuit for the non-inverting operational amplifier is shown in Fig. 2 In this circuit the signal is applied to the non-inverting input of the op-amp. However, the feedback is taken from the output of the op-amp via a resistor to the inverting input of the operational amplifier where another resistor is taken to ground. It is the value of these two resistors that govern the gain of the operational amplifier circuit. The output voltage equation of this amplifier

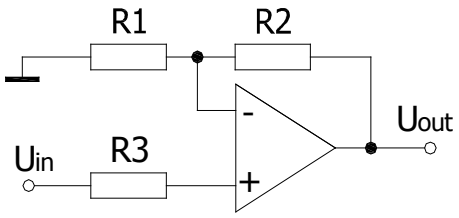

Fig 2. **Non-inverting operational amplifier circuit**

$$U_{out} = K_{OP}U_{in} \pm U_{0out}$$

where U_{0out} – zero offset voltage.

K_{OP} – static gain.

In the first approximation

$$K_{OP} = (1 + R_2 / R_1)\frac{K_G\beta}{1 + K_G\beta} \quad (1)$$

where K_G – signal amplification factor;

β – negative feedback transfer factor;

$$\beta = \frac{1}{1 + R_2 /(R_1 \| (R_3 + Z_{inOP}))}; \quad (2)$$

$$U_{0out} = (1 + R_2 / R_1)U_{offset} + \Delta I_{inOP}R_2; \quad (3)$$

in the second approximation

$$U_{0out} = (1 + R_2 / R_1)\frac{1}{1 + 1/K_G\beta}(U_{in} / K_{sf} + \Delta I_{inOP}(R_3 + R_s) +$$

$$+ \Delta I_{inOP}(R_3 + R_s + R_1 \| R_2) + K_P\Delta E_S + U_{sh}),$$

where K_P, U_{sh}, K_G, U_{offset}, I_{inOP}, ΔI_{inOP}, Z_{inOP}, Z_{outOP} – operational amplifier parameters;

ΔE_S – the operational amplifier supply voltage deviation;

$\|$ – mark of the parallel-connected elements;

R_s – signal source output resistance.

From the expression (1) follows that the amplifier gain factor can not be less than one. Besides, according to the equation (3), zero offset voltage is dependent on the input voltage level.

Input impedance:

$$Z_{in} = R_3 + Z_{inOP}(1 + K_G\beta). \quad (4)$$

Output impedance:

$$Z_{out} = Z_{outOP} /(1 + K_G\beta). \quad (5)$$

The maximum input voltage level is limited by the operational amplifier allowable phase synchronous voltage.

Capacitor charging and discharging with in series connected resistor. [1] The described scheme is shown in Fig. 3. While at the moment $t = 0$ the moving contact of the switch is connected to the DC source (clip 1). The capacitor before switching was not charged. First, the transition process, voltage, u_C and the current i must be found. According to the Kirchhoff law $u_a + u_C = U$, considering $u_a = R_1 i$ and $i = C\frac{du_C}{dt}$ differential equation for voltage u_C can be obtained:

$$R_1 C \frac{du_C}{dt} + u_C = U_{in}. \tag{6}$$

Following equation solution expressible $u_C = u_{C,free} + u_{C,\,forced}$, where $u_{C,\,forced} = U_{in}$, because the stationary mode is achieved at the moment when the capacitor I s charged to the source voltage.

The characteristic equation is $R_1Cp + 1 = 0$, from where $p = -(R_1C)^{-1}$. In the free mode $u_{C,free} = Ae^{-t/\tau}$, where $\tau = R_1C$ – time constant.

Inserting $t = 0$ into $u_{C,free}$ equation, to determine the integrating constant A we get expression $A = u_{C,free}(0) = u_C(0) - u_{C,\,forced}(0)$. In accordance with the second commutation law for non-charged capacitor $u_C(0) = -u_C(-0) = 0$. Then $A = -u_{C,\,forced}(0) = -U_{in}$. As a result we get the capacitor voltage during the transition process

$$u_C = u_{C,forced} + u_{C,free} = U_{in}(1 - e^{-t/\tau}). \tag{7}$$

The following expression is obtained for current:

$$i = C\frac{du_C}{dt} = -CU_{in}(-\frac{1}{\tau})e^{-t/\tau} = \frac{U_{in}}{R_1}e^{-t/\tau}. \tag{8}$$

If we compare this expression with the transition process of R and L series circuit, it is obvious, that the expression (7) is similar to the inductive current expression. Only the factor behind the brackets is different (it defines the unit of measurement) as well as the value of τ. This result is explained by the fact that the commutation law refers to u_C, under which its value changes from zero non-leap to the forced mode value.

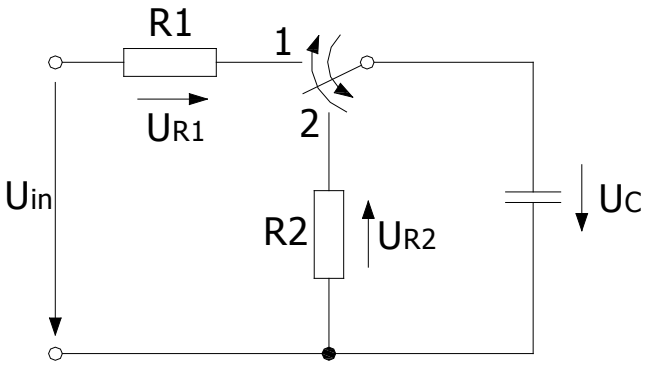

Fig. 3. **Capacitor charging and discharging circuit**

Assuming further that the circuit in Fig. 3. after the first switching practically achieved in forced mode switch switches to the second position, the capacitor starts to discharge through R_2 and short circuit, that is set up in stead of source. For simplicity it is assumed that $t = 0$ at the moment of the second switching. Then, before switching $u_C(-0) = U_{in}$, as determined by the previous transition process forced mode. In the new process again $u_C = u_{C,free} + u_{C,\,forced}$, where $u_{C,\,forced} = 0$, this time, because the process should end with a full capacitor discharge.

The differential equation of this circuit differs from the equation (6) only with the right hand side, but as the characteristic equation has to be written only as a homogeneous differential equation, then the characteristic equation and its root $p = -(R_2C)^{-1}$ remains unchanged. So $u_{C,free} = A_1e^{-t/(RC)} = A_1e^{-t/\tau}$, where a constant $A_1 = u_{C,free}(0) = u_C(0) - u_{C,\,forced}(0) = U_{in} - 0 = U_{in}$.

So the capacitor voltage during the transition process $u_C = u_{C,free} = U_{in}\,e^{-t/\tau}$ and current $i = C\frac{du_C}{dt} = -\frac{U_{in}}{R_2}e^{-t/\tau}$.

As shown, the voltage u_C again without hopping starts to evolve from the U_{in} value, and progressively tends to zero, but the current in the form of hopping is changed from zero to the value of $-U_{in} R_2^{-1}$, and also tends to zero and all time remains negative. This is also understandable because the actual discharge current direction is opposite to the presumed direction in Fig. 3. The charge and discharge curves are linked together in Fig. 4 a.

If the discharge of the capacitor should be started before it reached the connected voltage U_{in}, the second switching event would change only in the value of $u_C(-0)$. In the expression that describes the transition process after the first switching, nothing will change, because this process $u_{C,\ forced} = U_{in}$ regardless of whether that value is or is not reached. This transition process linked curves are showing Fig. 4 b.

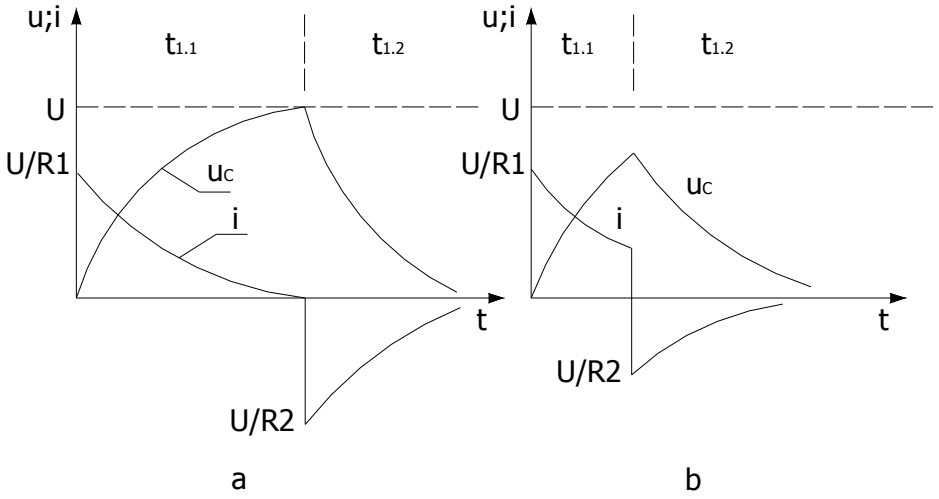

Fig. 4. **Capacitor charging and discharging curves**

Integrator reset circuits. [2] Integrator reset usually is performed discharging integrative capacity through the switch. As a switch typically relays and field effect transistors and optrons are used. While the integrator is reset, it is required that the integrator input is earthed or blocked. Fig. 5 shows two integrator reset circuits with field effect transistors that have been used as switches. Circuit, which appears in Fig. 5, at a closed switch V1 leakage current from the initial OP inlet passes through the transition drain - source, resulting in the integration error.

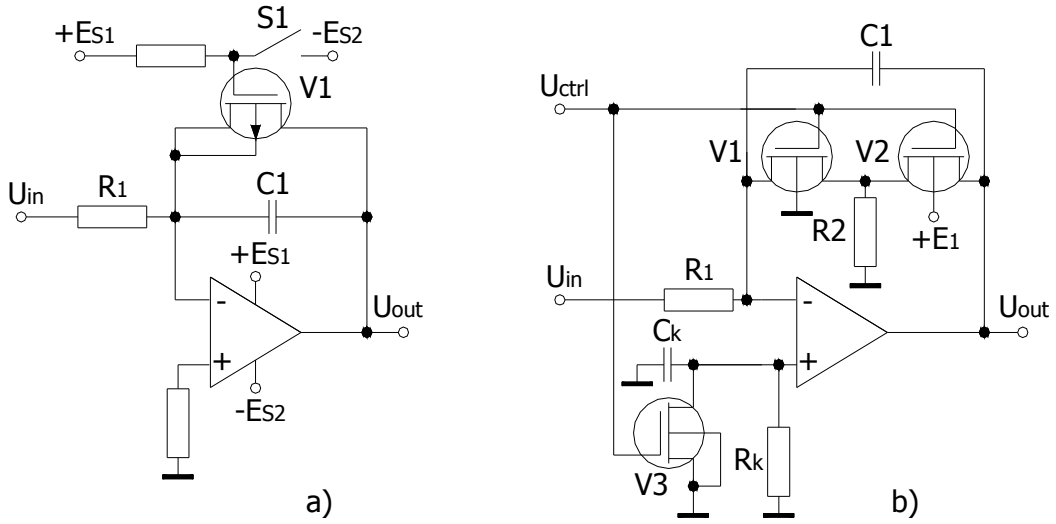

Fig. 5. **Integrator reset circuits:** a – with field effect transistor switch, b – with field effect transistor lekage current compensation

To reduce leakage currents drain - source, there can be used two in a series switches, for the circuit shown in Fig. 5 b. Here is no leakage, which comes through the switch summing point transition drain - source, because at the closed switches V1 and V2, the leakage current from the OP2 output through the transition drain - source V2 is discharged to the ground through relatively small resistance R2. Since the capacitor C1 is set to a short circuit it can occur that OP input current displaced, so the resistor R_k must be grounded. At the same time, connecting parallel capacity $C_k = C_1$ with resistor R_k it is possible to compensate pulse distortions that occur during switching.

Pulse density modulation circuit operation. Figure 6 is given to explain PDM circuit operation. At time $t = 0$, the capacitor and the signal voltage is zero. Next the capacitor begins charging, because the signal voltage U_{in} is increasing, the capacitor voltage reaches the comparison voltage $U_{stabilised}$ (Fig. 1) value at the time $t = t_{1.1}$. This curve of this process is shown in Fig. 4 b $t_{1.1}$ interval.

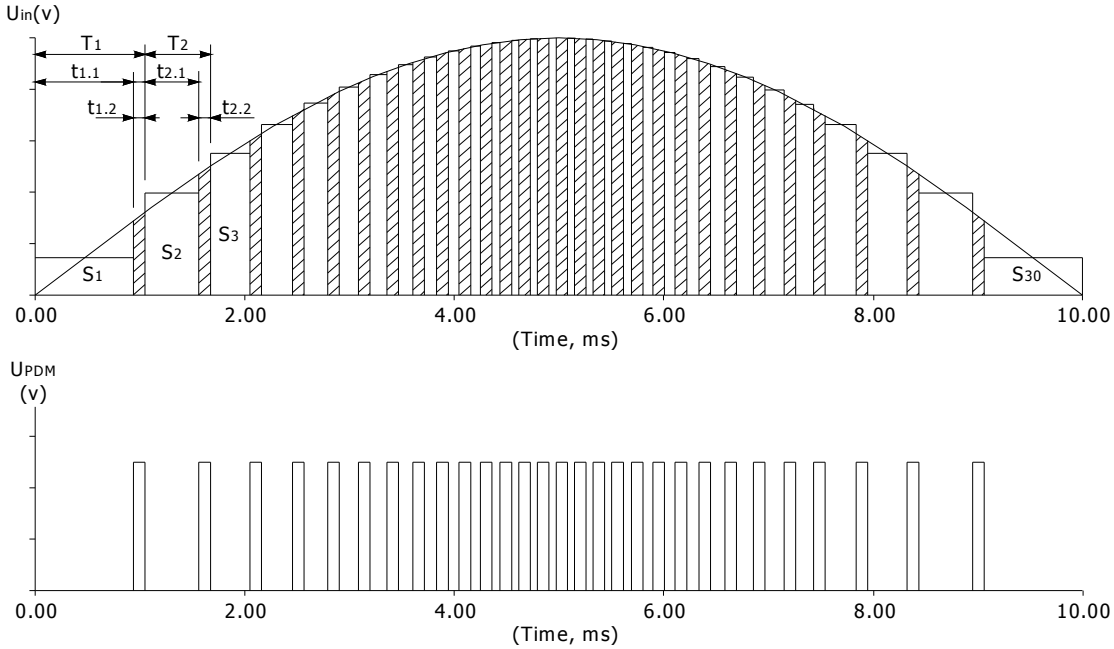

Fig. 6. **Pulse density modulation circuit operation**

Now, when the capacitor voltage and $U_{stabilised}$ are equal, the capacitor discharge control switch is activated by the impulse, the capacitor is being discharged through the resistor, the same impulse is transferred to the output as U_{PDM} (Fig. 6). A new capacitor charging and discharging period begins, which differs from the previous by the fact that the capacitor charging voltage is higher level, thus it will reach $U_{stabilised}$ value faster. The capacitor discharge time does not change, because the discharge conditions remain the same. At higher input voltage U_{in} circuit obtains higher impulse $t_{1.n}$ proportion against blanks $t_{2.n}$ during period T_n.

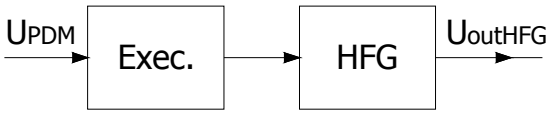

Fig. 7. **Pulse package generation**

Forming of power AC. The high frequency generator HFG is operated by PDM circuit. During each U_{PDM} pulse HFG generates 20 kHz pulse packages (Fig. 7, Fig. 9). The HFG operating principle is the following, switches are switched by pairs S1, S3 and S2, S4 synchronously contrary. When S1 and S3 are turned on, S2 and S4 are off, this way high frequency voltage form is generated using DC energy stored by the capacitor (Fig 8).

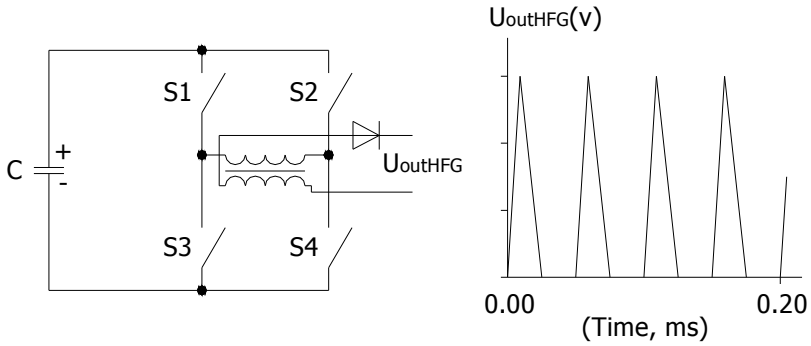

Fig. 8. **High frequency power generator**

Results and discussion

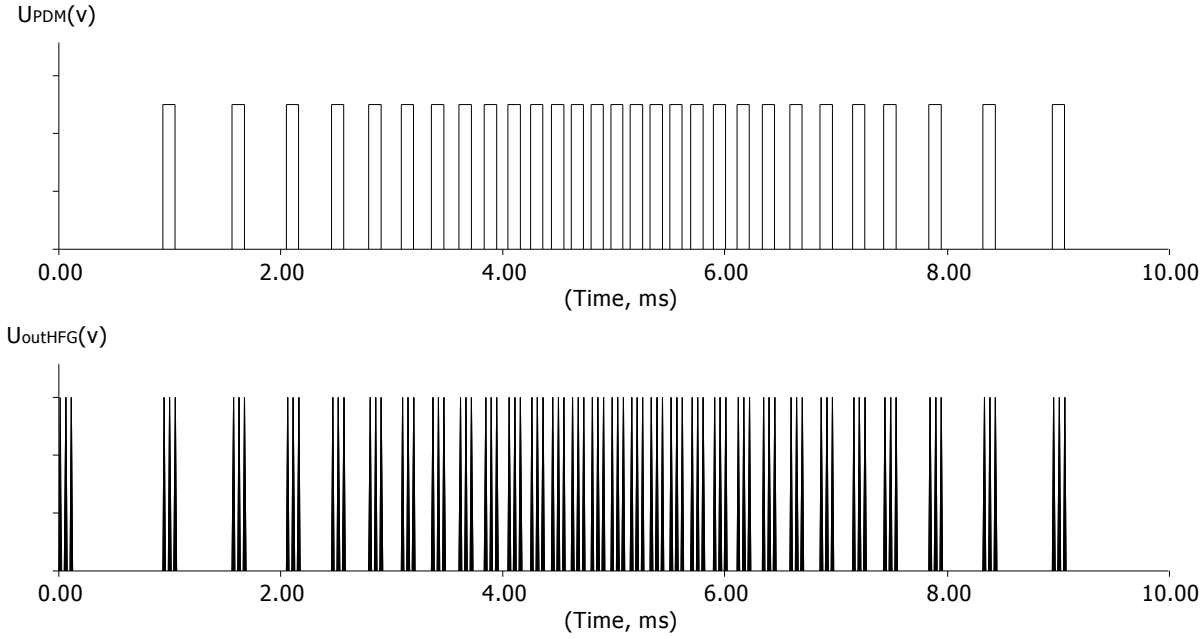

Fig. 9. **Forming of power AC**

The pulse density modulation circuit is developed, which generates fewer constant length pulses at lower input voltage, increasing the input voltage, the output pulse count per time unit on circuit output increases, in addition the pulse length remains fixed (Fig. 7). Every output pulse blocks the input signal at its corresponding moment, to escape the capacitor charging and discharging simultaneously. Output pulses are differenced to the desired amplitude so PDM circuit is suitable for use as a power electronics control circuit.

Comparing the PDM method with the pulse width modulation (PWM) method, PDM is able to give much less harmonic spectrum. PDM is applicable to the voltage shape distortion reduction system. Comparing the actual load voltage with the required voltage the PDM method can compensate the load voltage with positive or negative pulse packages depending on the load voltage and the required voltage comparison result.

PDM frequency can be adjusted changing the integrator capacity. Increasing the integrator capacity, the frequency of PDM reduces, reducing the capacity its frequency is increasing. The pulse length can also be regulated, it extends by increasing the integration capacity discharge branch resistance, and the pulse length is extended by reducing this resistance.

Conclusions

1. The resulting circuit obtained is applicable in power electronics as a control unit to form AC curve voltage.
2. PDM circuit output parameters can be adjusted such as PDM frequency and pulse length.
3. PDM gives less harmonic spectrum than PWM.
4. PDM method is applicable to the voltage shape distortion reduction system.

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